IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Richard Nathan		
Assignee:	JigSaw Tek		
Title:	Integrated Circuit Package and Method for Fabricating		
Serial No.:	10/077,211	Filing Date:	Feb. 14, 2002
Examiner:	David A. Zarneke	Group Art Unit:	2827
Docket No.:	JIG006 US	Confirmation No:	3098

Santa Clara, California
October 31, 2003

COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.97(c)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, §1.97 and §1.98, the Applicants submit for consideration in the above-identified patent application the documents listed on the accompanying Form PTO-1449. Copies of the documents 17, 37-39 are also submitted herewith. The Examiner is requested to make these documents of record.

This Information Disclosure Statement is submitted pursuant to 37 CFR §1.97(c) as it is after receipt of a first Office Action on the merits but before mailing of a final Action or Notice of Allowance. Accordingly, a fee is required pursuant to 37 CFR §1.17(p). A Fee Transmittal form (PTO/SB/17) is attached to this submission.

Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

In addition, Applicants submit for the Examiner's consideration the following list of co-pending and co-owned applications, cited by serial number, first named inventor and filing date. The Applicants presume that the Examiner has access to and will review the co-pending applications and the files thereof for any office actions, amendments or other

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materials that may be relevant to the patentability of the claims of the present application. For any such U.S. patent application(s) that are currently pending, the Applicants further presume that the Examiner will consider any future office actions, amendments or other materials in the file thereof that may be relevant to the patentability of the claims herein. **If the Applicants' understanding in this regard is not correct, please notify the undersigned so that copies of any such documents can be submitted to the Examiner.**

	Serial No.:	First Named Inventor	Date:
1.	10/177,841	Richard Nathan	6/20/02
2.	10/098,021	Richard Nathan	03/12/02
3.	09/953,005	Richard Nathan	9/13/01
4.	10/097,363	Richard Nathan	03/12/02

The information contained in this Information Disclosure Statement is to the best of my knowledge and is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office to the fax number 703-872-9318 on October 31, 2003.

S. Omkar — Oct 31, 2003

Attorney for Applicant(s) — Date of Signature

Respectfully submitted,

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(Use several sheets if necessary)	Group Art Unit:	2827
	Examiner Name:	David A. Zarneke
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	Attorney Docket No.:	JIG006 US

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	1.	5,313,366	5/17/94	Gaudenzi et al.	361	760	
	2.	5,701,233	12/23/97	Carson et al.	361	735	
	3.	5,756,368	05/26/98	Peterson et al.	438	110	
	4.	6,175,161	01/16/01	Goetz et al.	257	780	
	5.	5,375,041	12/20/94	McMahon	361	749	
	6.	5,821,762	10/13/98	Hamaguchi, et al.	324	754	
	7.	5,556,807	9/17/96	Bhattacharyya et al.	437	209	
	8.	6,307,450	10/23/01	Takahashi et al.	333	204	
	9.	5,815,372	9/29/98	Gallas	361	760	
	10.	5,488,257	1/30/96	Bhattacharyya et al.	257	774	
	11.	6,130,478	10/10/00	Dumoulin et al.	257	728	
	12.	5,608,262	03/04/97	Degani et al.	257	723	
	13.	6,075,427	06/13/00	Tal et al.	333	219	
	14.	5,880,529	03/09/99	Barrow	257	782	
	15.	5,976,980	11/02/99	Livengood et al.	438	691	
	16.	4,918,811	04/24/90	Eichelberger et al.	438	107	

Foreign Patent Documents

		Document	Date	Country	Name	Classification
	17.	52-30390	03-1977	Japan	Yoshikaza	27/04

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	18.	6,528,351	03/04/03	Nathan et al.	438	118	
	19.	5,032,896	07/16/91	Little et al.	257	686	
	20.	5,745,984	05/05/98	Cole Jr. et al.	29	834	
	21.	5,949,133	09/07/99	Wojnarowski	257	668	
	22.	6,204,095	03/20/01	Franworth	438	127	
	23.	4,722,914	02/02/98	Drye et al.	438	107	
	24.	6,309,912	10/30/01	Chiou et al.	438	126	
	25.	5,353,498	10/11/94	Fillion et al.	29	840	
	26.	5,188,984	02/23/93	Nishiguchi	438	107	
	27.	5,982,632	11/9/99	Mosley et al.	361	775	
	28.	6,147,876	11/14/00	Yamaguchi et al.	361	766	
	29.	6,162,652	12/19/00	Dass et al.	438	18	
	30.	6,229,216	05/08/01	Ma et al.	257	777	
	31.	6,333,210	12/25/01	Dubey et al.	438	108	
	32.	5,378,657	01/03/95	Lin	437	217	
	33.	4,735,891	04/05/88	Budde et al.	430	313	
	34.	6,222,737	04/24/01	Ross	361	767	
	35.	2002/0185734 A1	12/12/02	Zhao et al.	257	737	
	36.	6,137,129	10/24/00	Bertin et al.	257	302	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	37.	Mahajan, Ravi et al., "Emerging Directions For Packaging Technologies", Intel Technology Journal, Volume 6, Issue 2, Published, May 16, 2002, ISSN 1535766X, Cover page plus pages 62-75.
	38.	Press Release, October 8, 2001, Santa Clara, CA, "Intel Researchers Disclose Packaging Technology Breakthrough to Enable Billion-Transistor Processors", 3 pages. http://www.intel.com/pressroom/archive/releases/20011008tech.htm.
	39.	Press Release, October 8, 2001, Santa Clara, CA, "Bumpless Build-up Layer Packaging Technologies", 3 pages, http://www.intel.com/pressroom/archive/backgrnd/20011008tech_bkgrd.htm.

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